

FIG. I

APPROVED	O.G. FIG.
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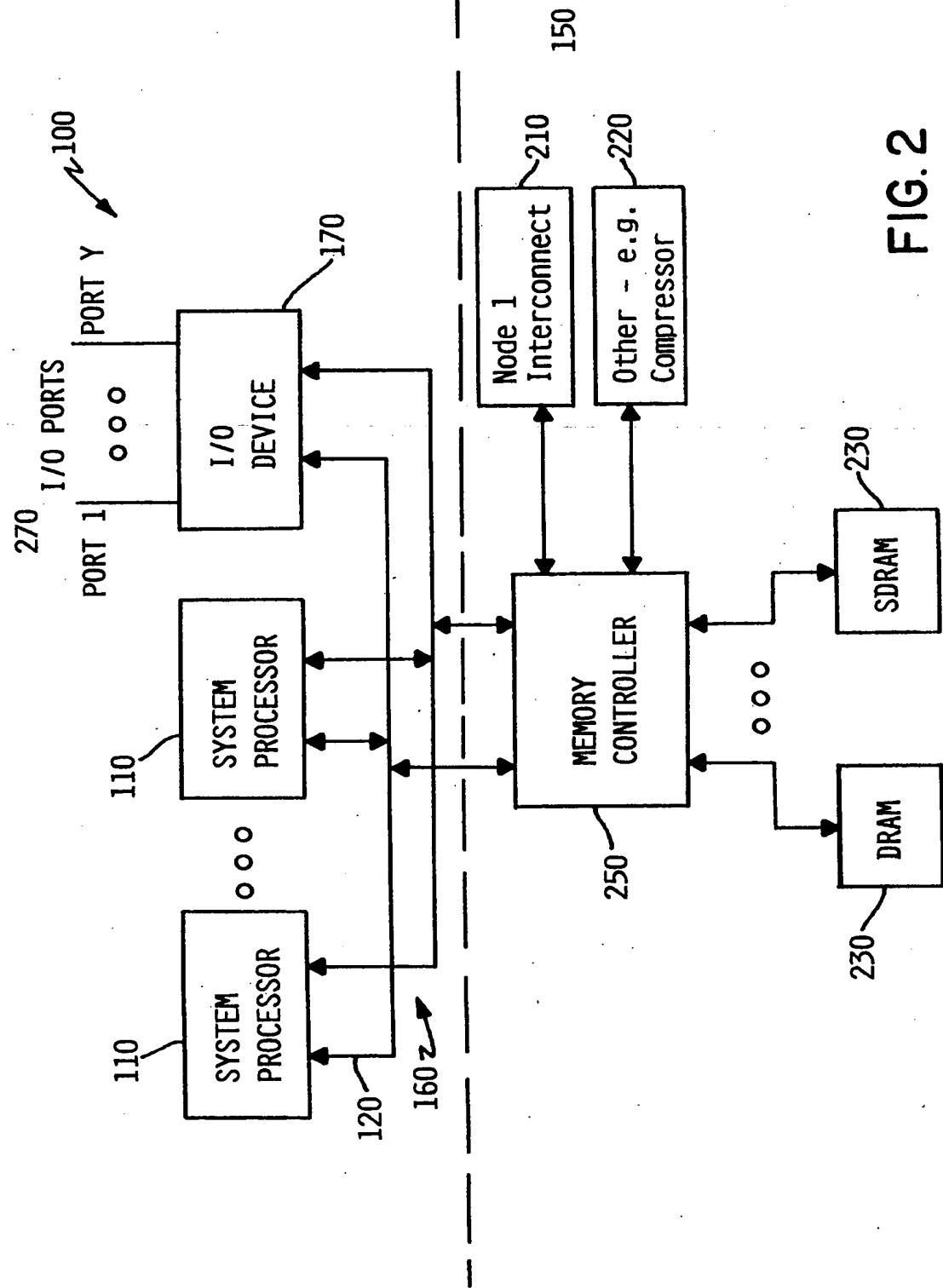
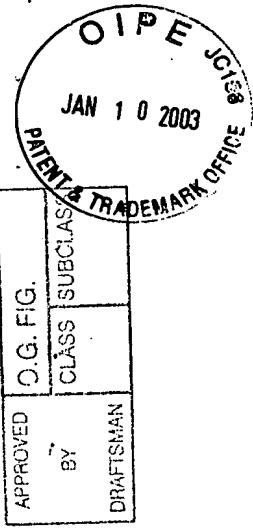


FIG. 2



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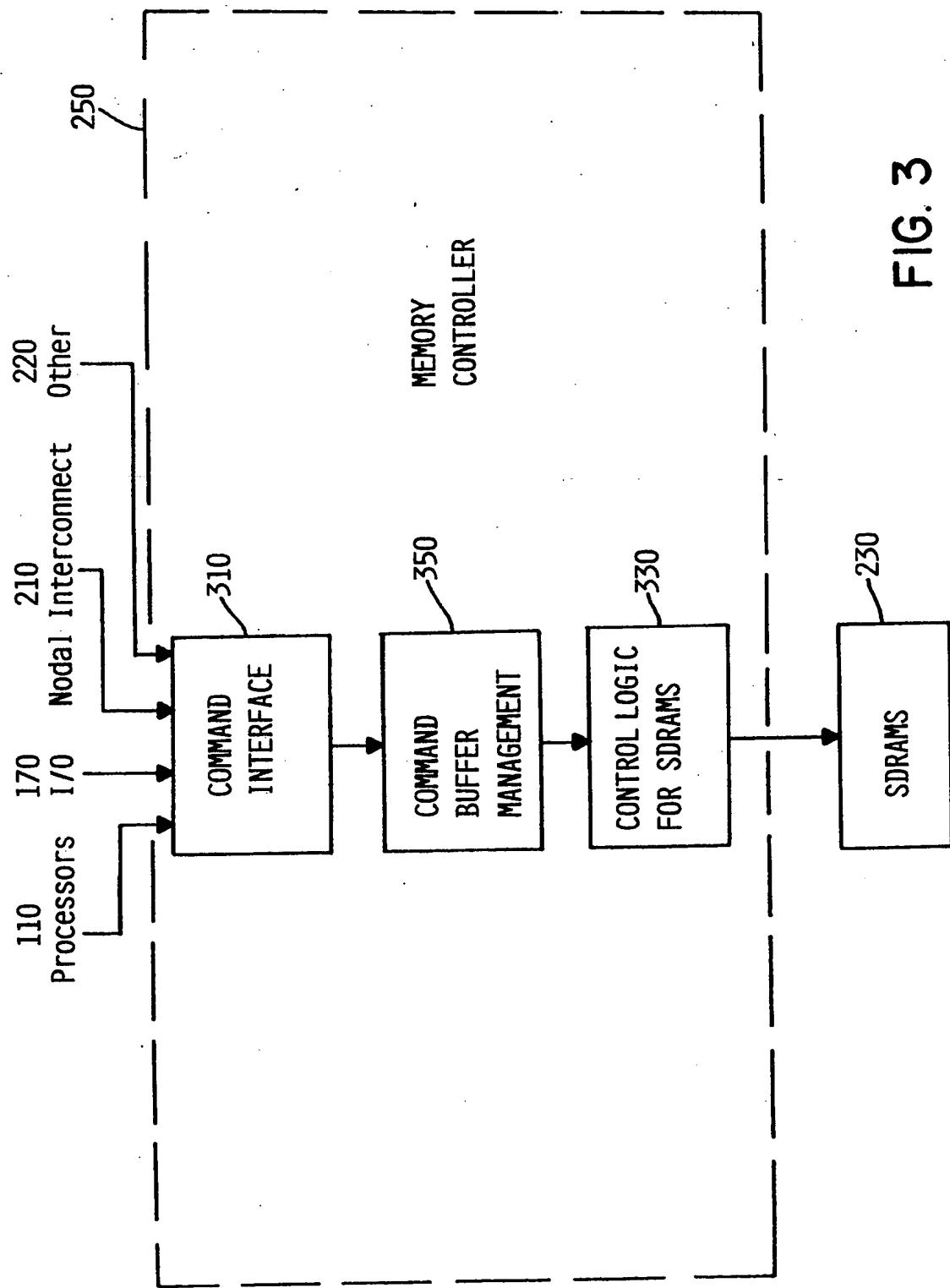
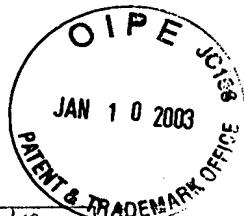


FIG. 3



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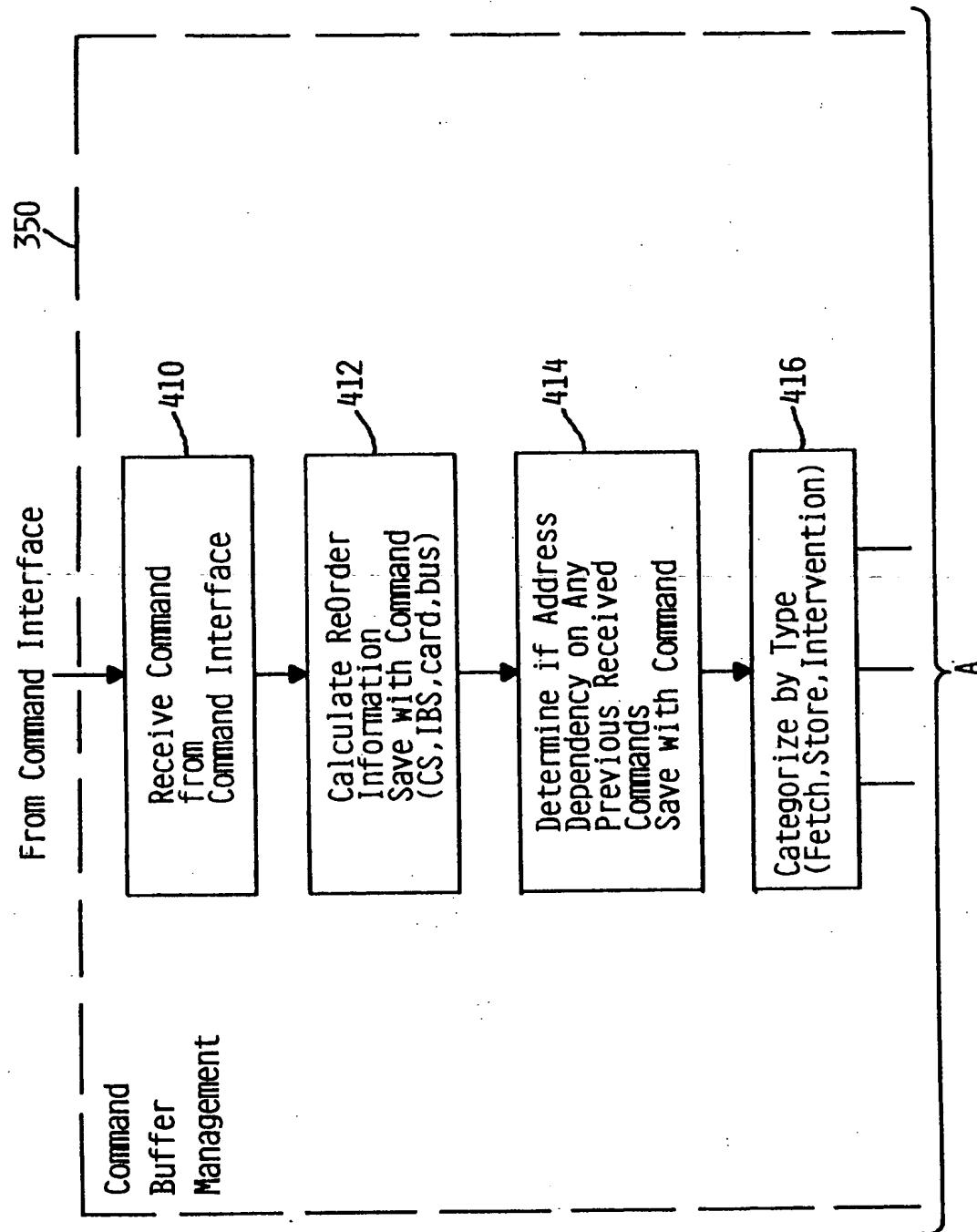


FIG. 4A



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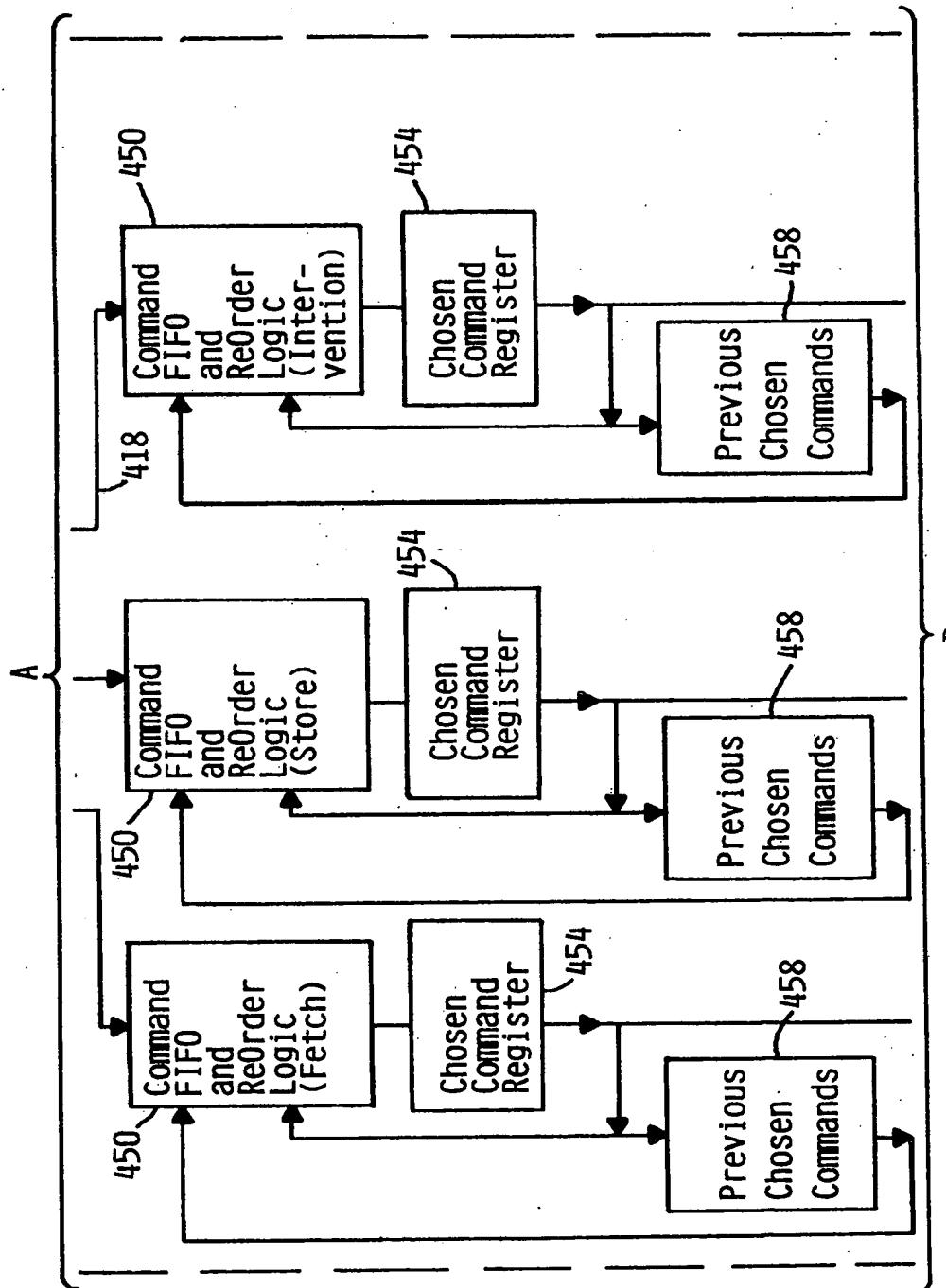


FIG. 4B



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APPROVED	D.G. FIG.
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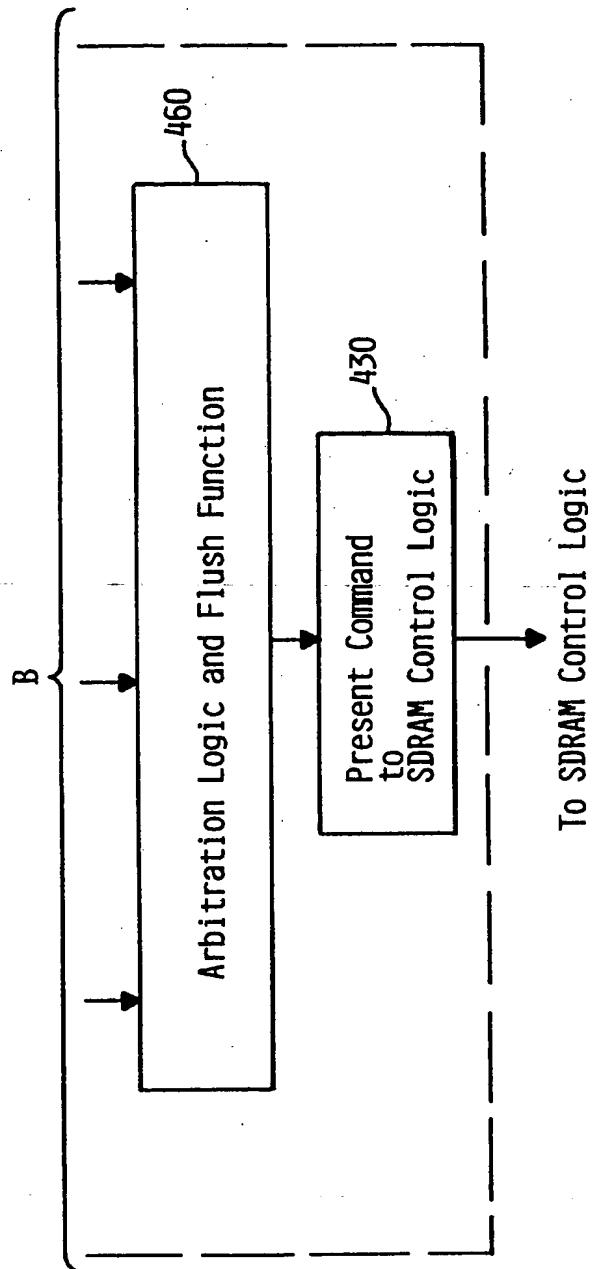
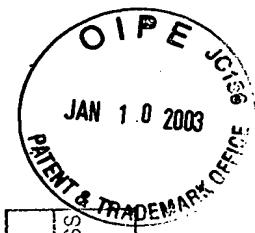


FIG. 4C



APPROVED	O.G. FIG.
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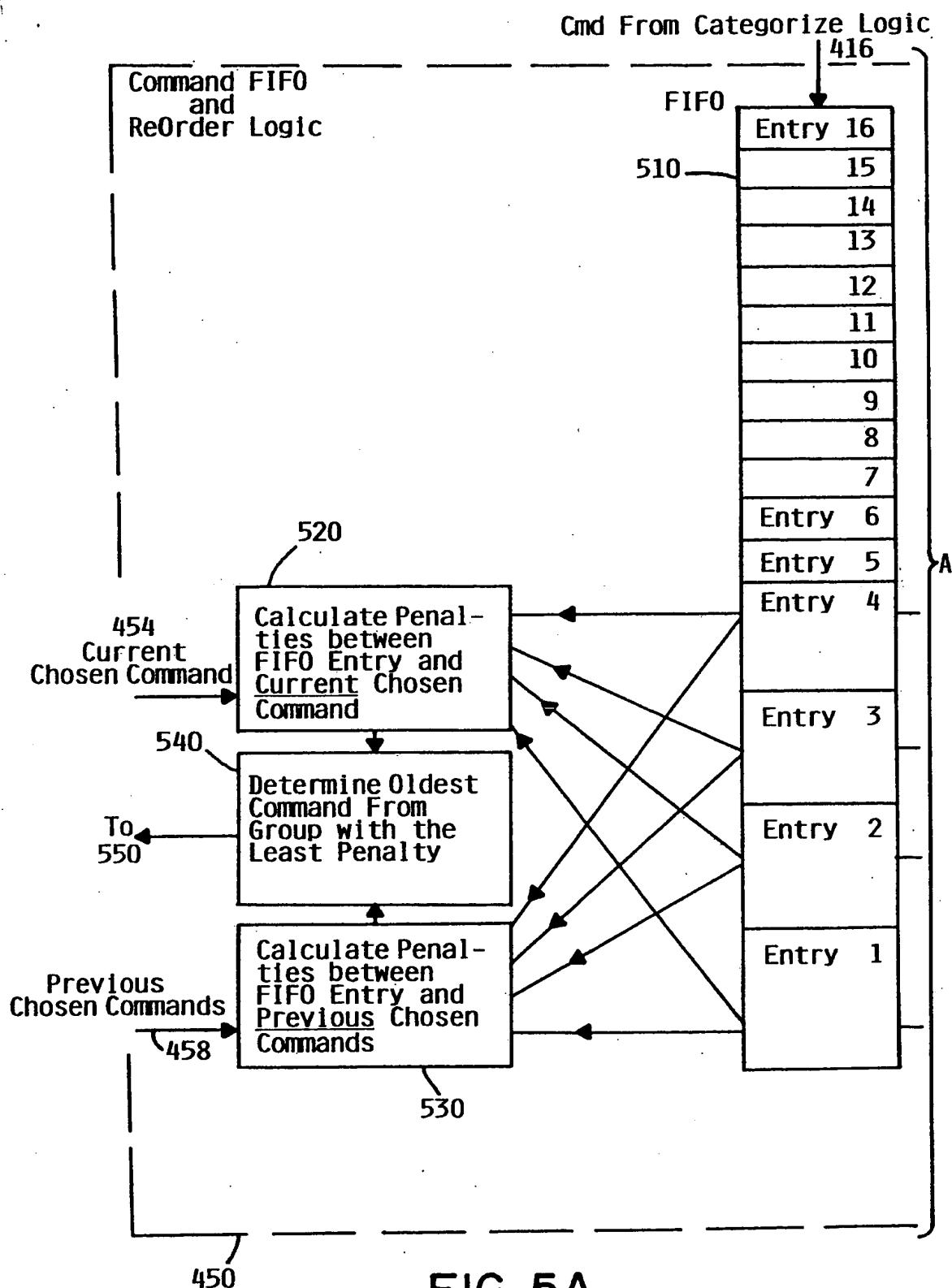
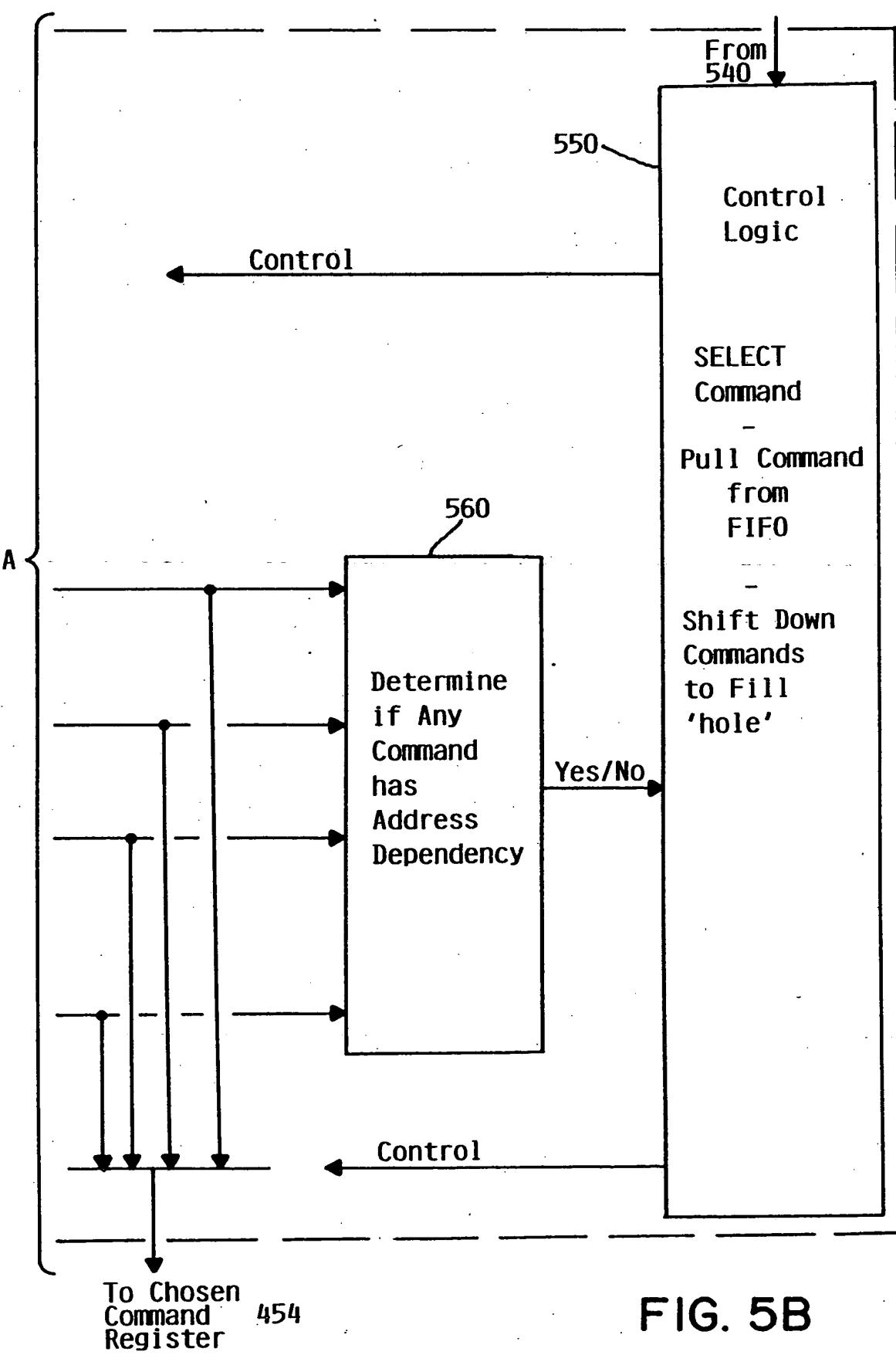


FIG. 5A



APPROVED	O.G. FIG.
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Command FIFO and Reordering - Flow Diagram

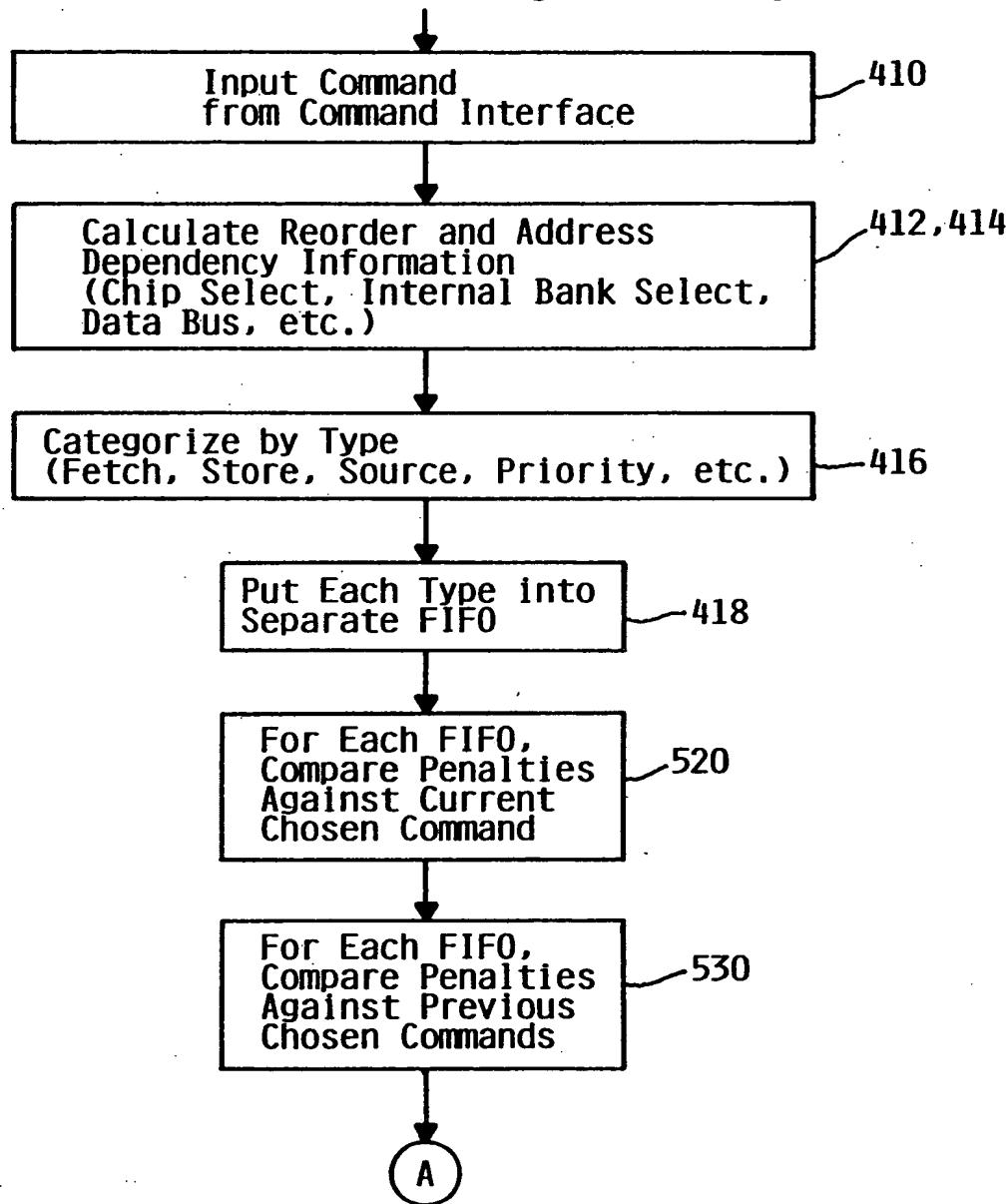


FIG. 6A



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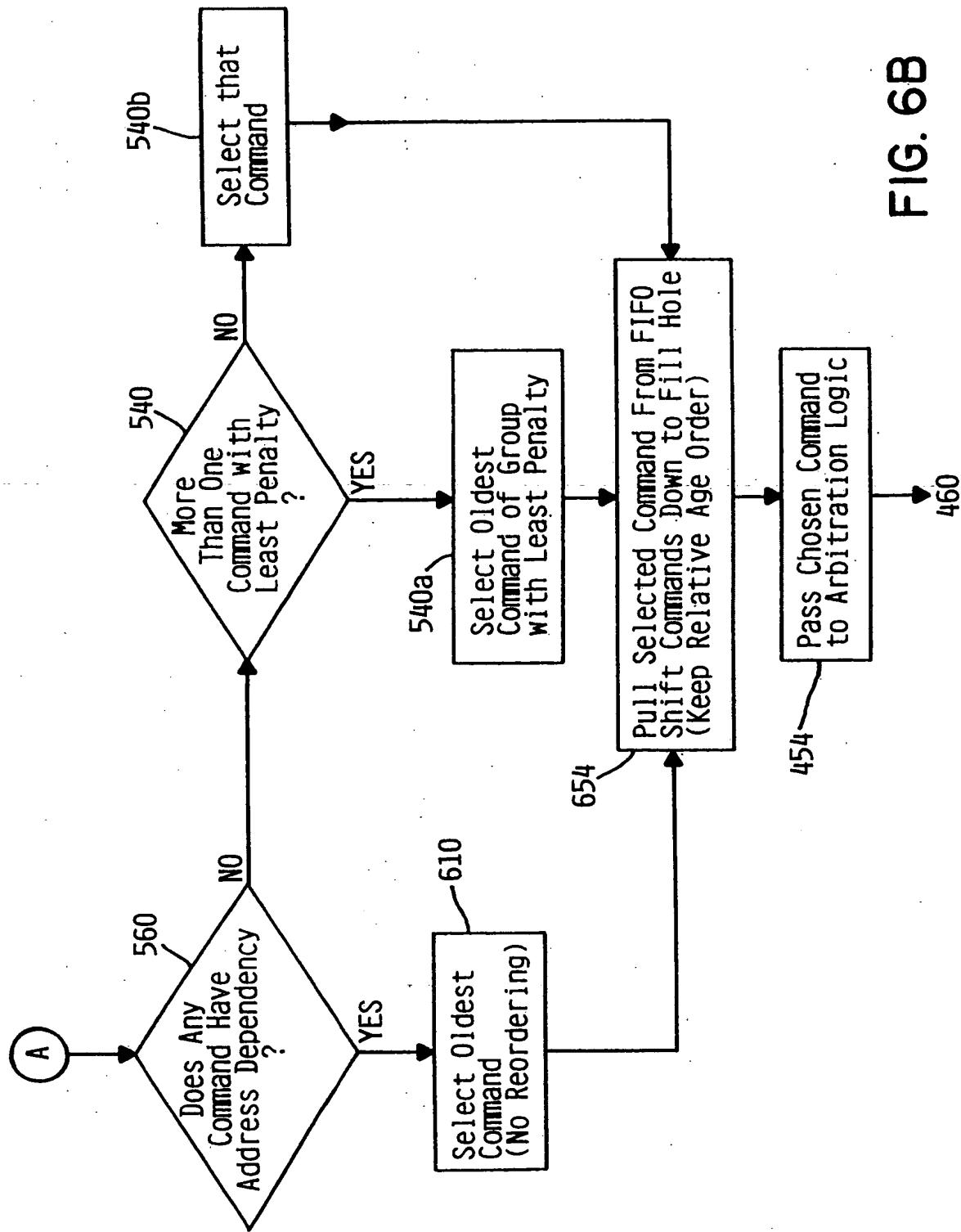


FIG. 6B



APPROVED	O. G. FIG.	
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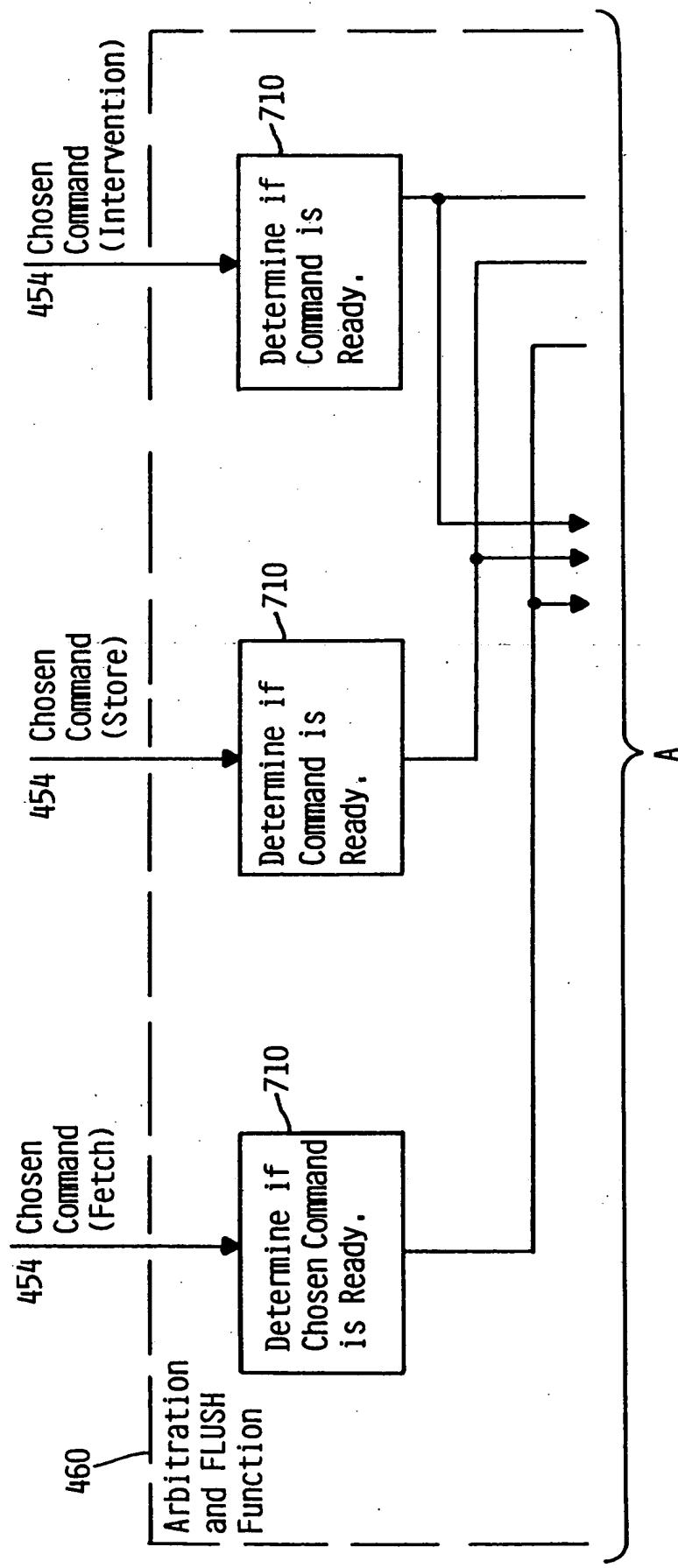


FIG. 7A

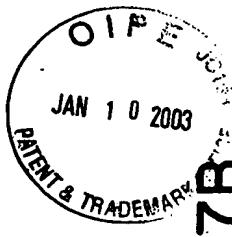
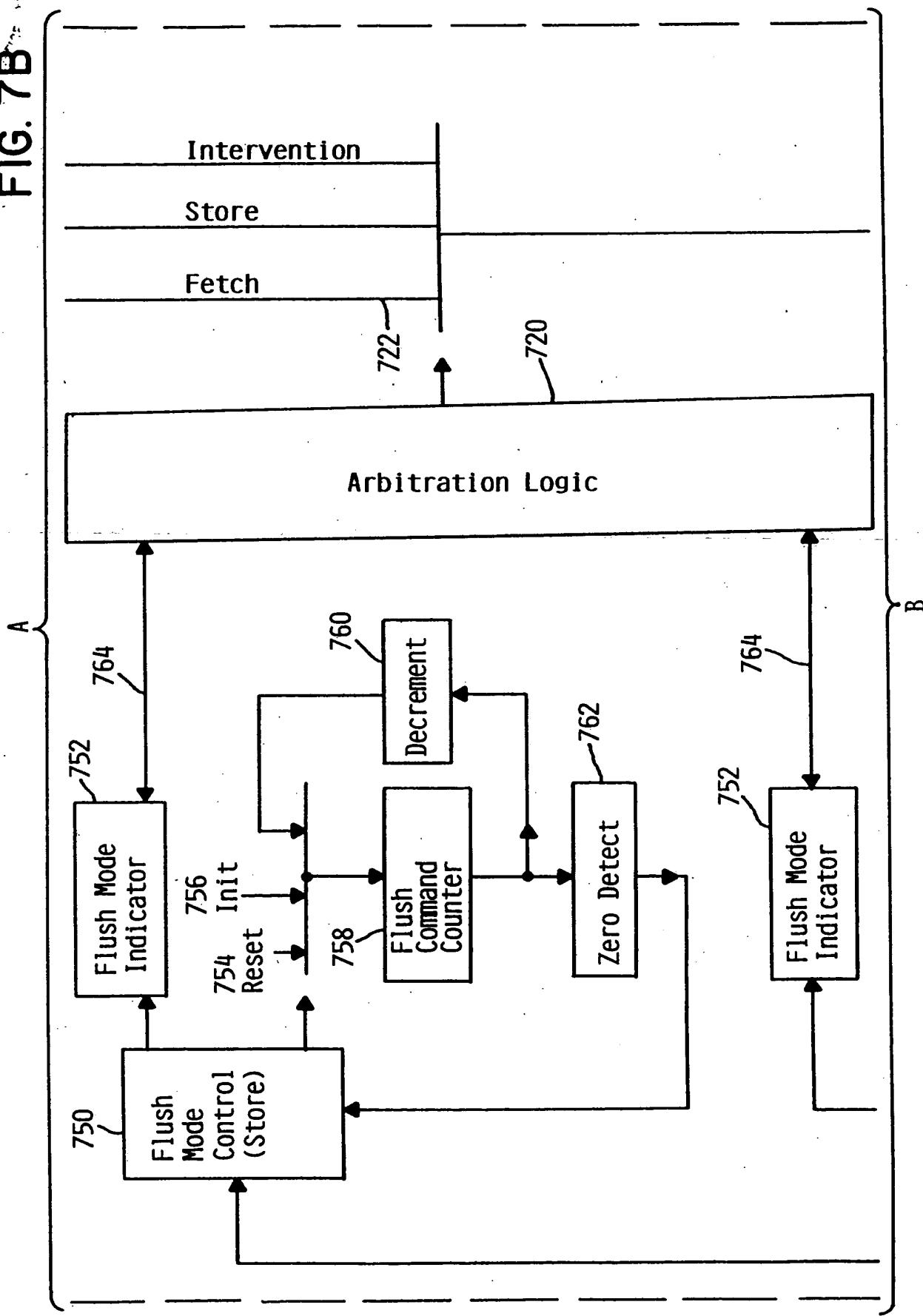


FIG. 7B





APPROVED	O.G. FIG.
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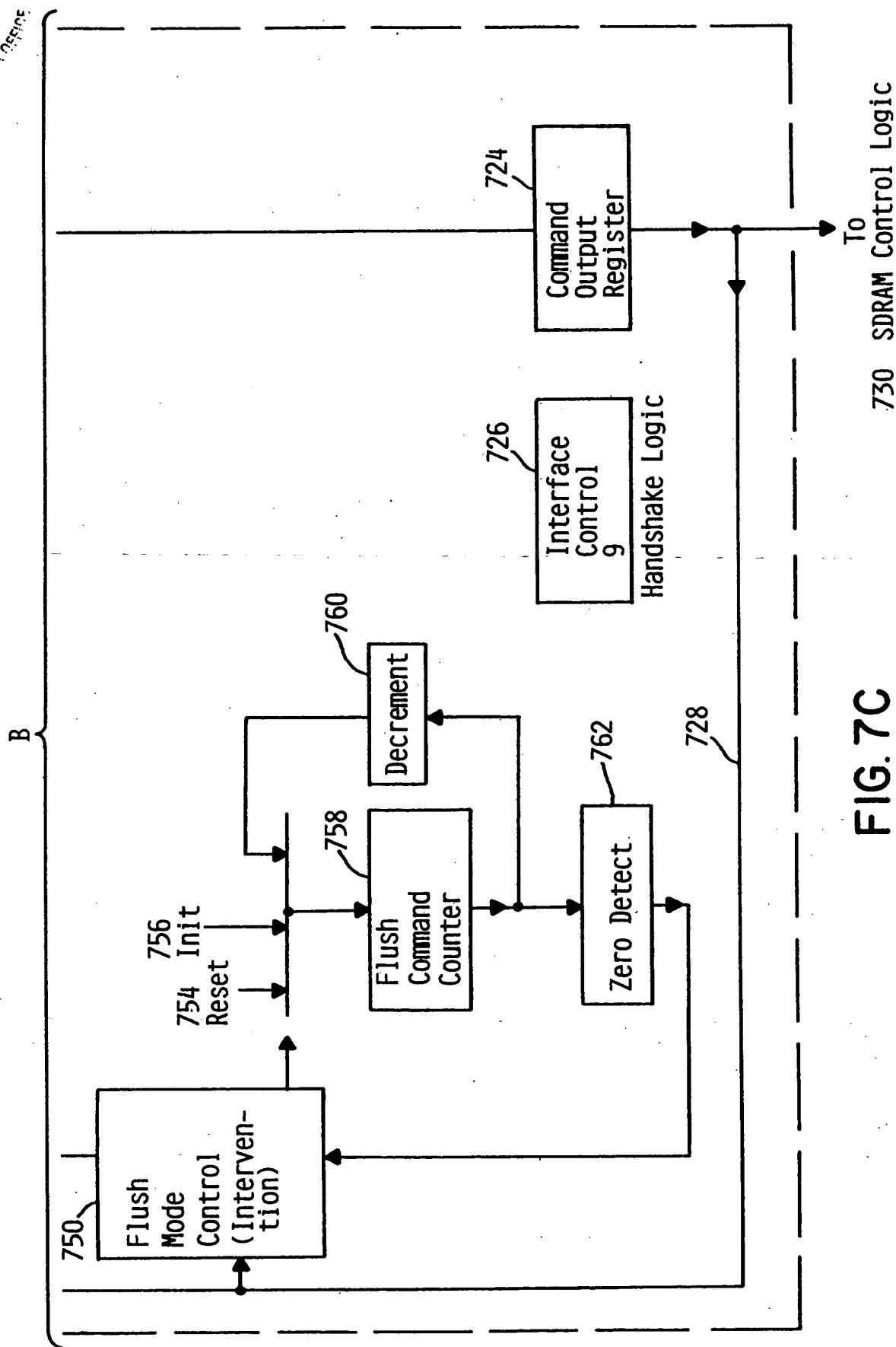
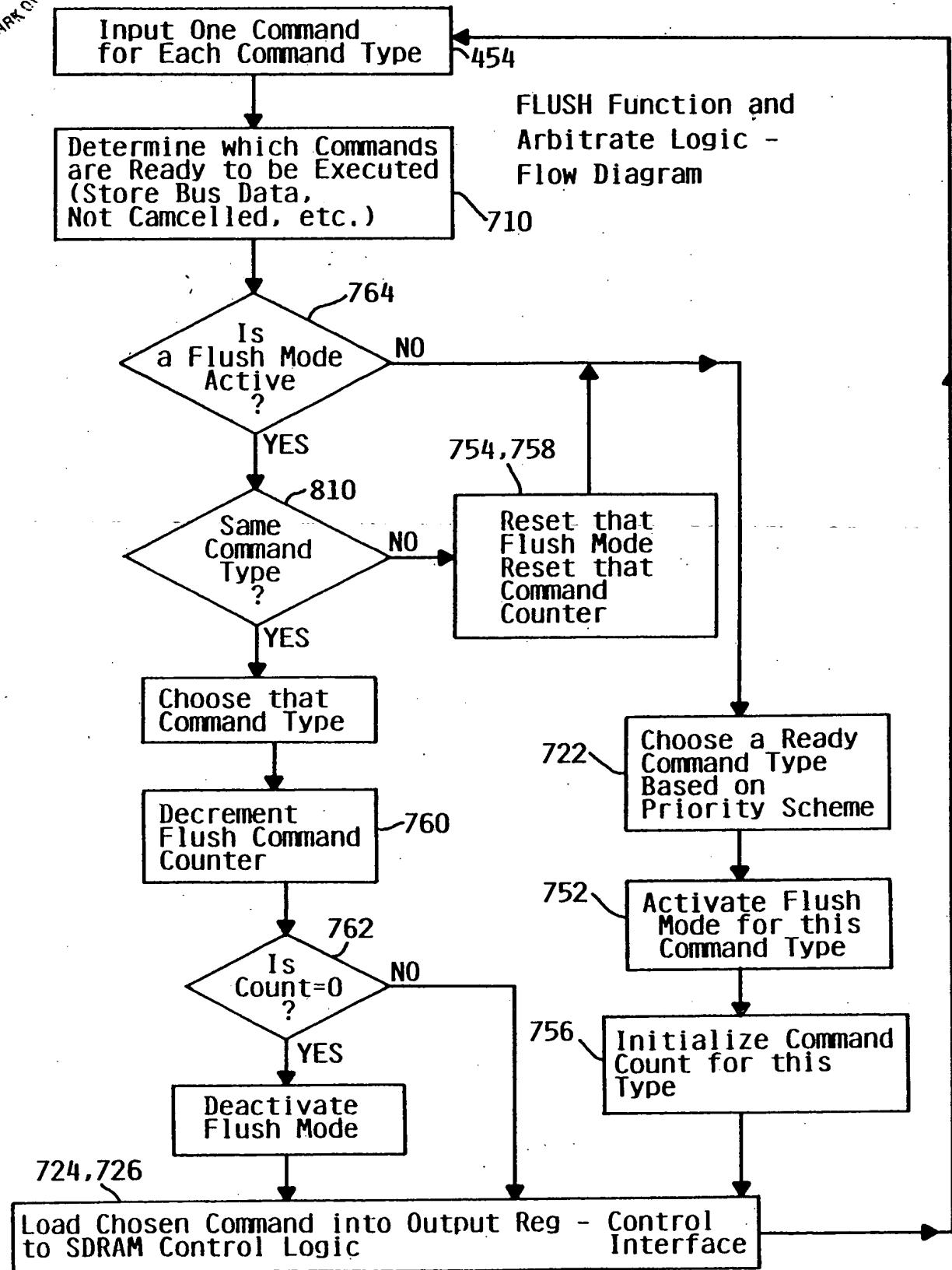


FIG. 7C

730 SDRAM Control Logic



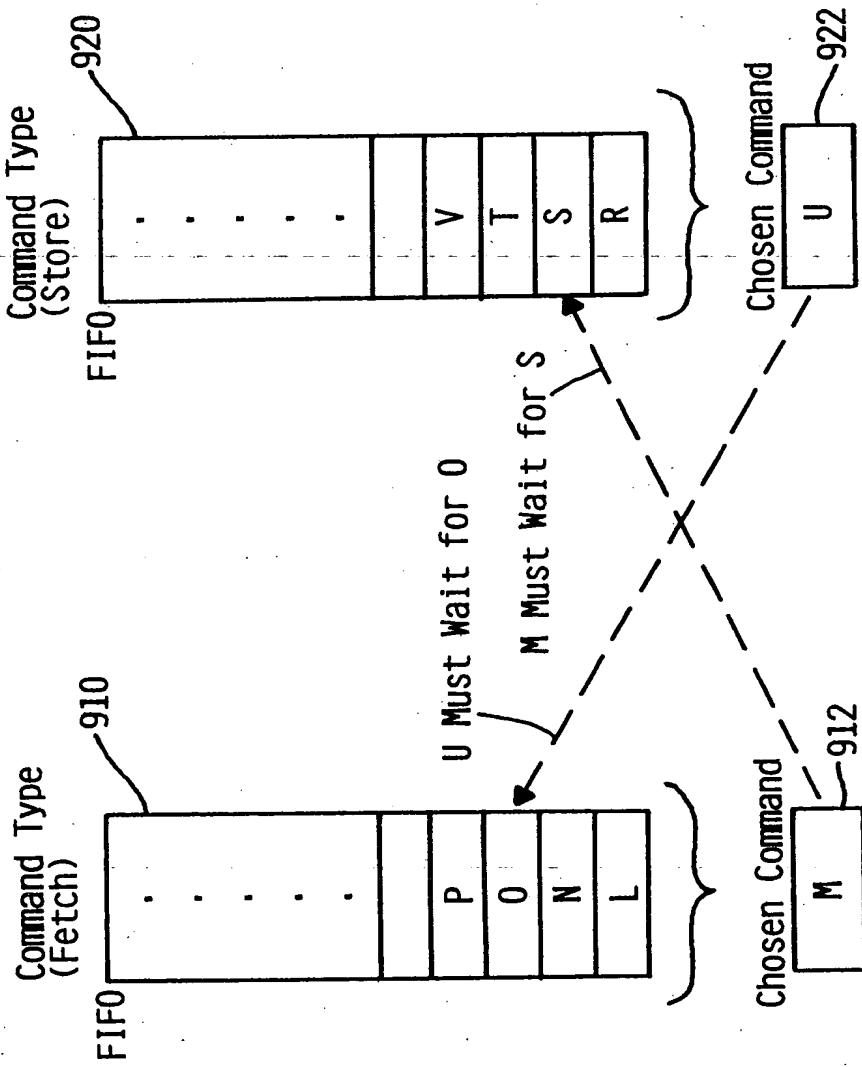
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**FIG. 8**



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Deadlock Condition - (occurred by ReOrdering)

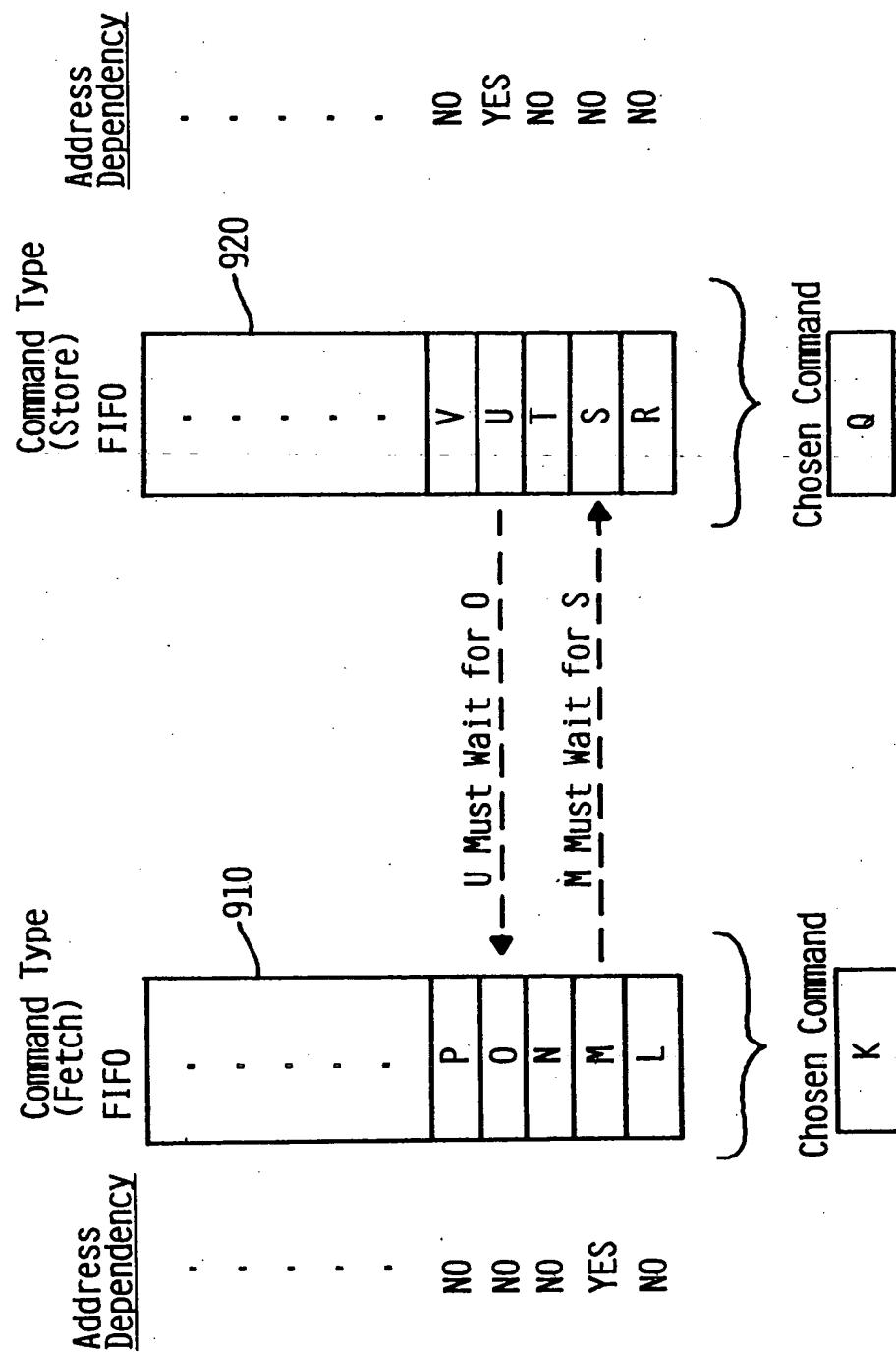


- * If certain command chosen by ReOrder Logic, then deadlock
 - Key idea is to not reorder if any command being considered has an address dependency

FIG. 9A



Possible Deadlock Condition - (Avoided by executing as FIFO)



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- Command U address is in same cache line as command 0, and was received after command 0.
- Command M address is in same cache line as command S, and was received after command S.
- * If commands in both FIFOs execute in order, then no deadlock.

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